Docket No.: 10017911-1-3-Streeter (1509-240A) PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented): A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, said first and second transistors being respectively a PFET and an NFET, each of said transistors including a gate electrode and a source drain path arranged to be switched on and off in response to a voltage applied to the gate electrode being on opposite sides of a threshold, the first and second transistor paths being connected in series across opposite power supply terminals, and pulse shaping circuitry for (a) causing the first and second source drain paths to be respectively (i) on and off while the voltage source has the first level and (ii) off and on while the voltage source has the second level, and (b) preventing both source drain paths from being on simultaneously, the pulse shaping circuitry including a resistive element and a capacitor, the resistive element being connected for supplying current to the capacitor and the gate electrode of the first transistor, the capacitor being connected across the gate electrode of one of said transistors and a first of the power supply terminals, the first power supply terminal being connected for supplying current to the source drain path of the other of said transistors while the source drain path of the other of said transistors is on, the capacitor comprising a field effect device having a conductivity type opposite to the conductivity type of said one of said transistors.

Claim 2 (canceled).

Claim 3 (previously presented): The circuit of claim 1 wherein said resistive element, PFET, NFET and said capacitor are included on an integrated circuit chip, and said resistive element comprises a resistor.

Claims 4-6 (canceled).

Claim 7 (previously presented): The circuit of claim 1 wherein the pulse shaping

circuitry includes a switching circuit having (a) an input terminal for enabling the switching circuit to be responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the switching circuit being connected so current can flow via a DC path between (a) the first power supply terminal and (b) the capacitor and the gate electrode of said one transistor, the DC path including the resistive element.

Claim 8 (previously presented): The circuit of claim 7 wherein the switching circuit includes an inverter having field effect transistors.

Claim 9 (previously presented): The circuit of claim 8 wherein all the field effect transistors of the inverter are included on an integrated circuit chip including a resistor comprising the resistive element connected with said one field effect transistor and the inverter.

Claim 10 (previously presented): The circuit of claim 9 wherein the resistor is included in the inverter.

Claim 11 (previously presented): The circuit of claim 10 wherein the inverter includes a PFET and an NFET, the PFET and NFET of the inverter having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the PFETs and NFETs of the inverter are arranged to be driven in parallel by the voltage at the first terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof.

Claim 12 (previously presented): The circuit of claim 11 wherein the resistor is connected between the source drain path of the NFET of the inverter and the output terminal of the inverter.

Claim 13 (canceled).

Claim 14 (previously presented): A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, each of the transistors including a control electrode and a path switched on and off in response to a voltage applied to the control electrode

being on opposite sides of a threshold, the first and second transistor paths being connected in series across opposite first and second power supply terminals, an output terminal between the paths, pulse shaping circuitry connected between the input terminal and the control electrodes for (a) causing the paths of the first and second transistors to be respectively (i) on and off while the voltage source has the first level and (ii) off and on while the voltage source has the second level, and (b) preventing the paths of the first and second transistors from being on simultaneously, the pulse shaping circuitry including: (a) first and second switching circuits arranged to be connected to be simultaneously responsive to the voltage at the first terminal, the first and second switching circuits respectively including output terminals that are DC connected to the control electrodes of the first and second transistors; and (b) first and second capacitors that are respectively DC connected between (i) the first control electrode and the first power supply terminal and (ii) the second control electrode and the second power supply terminal, the first switching circuit including a first resistive element for supplying current from the first power supply terminal to the control electrode of the first transistor and the first capacitor while the voltage at the first terminal has the first level, the first switching circuit being arranged for supplying a voltage substantially equal to the voltage at the second power supply terminal to (i) the control electrode of the first transistor and (ii) the first capacitor while the voltage at the first terminal has the second level; the second switching circuit including a second resistive element for supplying current from the second power supply terminal to the control electrode of the second transistor and the second capacitor while the voltage at the first terminal has the second level, the second switching circuit being arranged for supplying a voltage substantially equal to the voltage at the first power supply terminal to (i) the control electrode of the second transistor and (ii) the second capacitor while the voltage at the first terminal has the first level, the first switching circuit comprising: a first inverter including third and four transistors respectively connected to be switched on and off in response to the voltage at the first terminal respectively having first and second values, the first inverter including the first resistive element for supplying current from the first power supply terminal to the control electrode of the first transistor and the first capacitor while the third transistor is switched on; the second switching circuit comprising a second inverter including fifth and sixth transistors respectively switched on and off in response to the voltage at the first terminal respectively having first and second values, the second inverter including the second resistive element for supplying current from the second power supply terminal to the control electrode of the second transistor and the second capacitor while the sixth transistor is switched on, each of the inverters including a PFET and an NFET, the PFET and NFET

of each inverter having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the PFETs and NFETs of the inverters are arranged to be driven in parallel by the voltage at the first terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof, the first resistive element being connected between the source drain path of the NFET of the first inverter and the output terminal of the first inverter, the second resistive element being connected between the source drain path of the PFET of the second inverter and the output terminal of the second inverter.

Claim 15 (canceled).

Claim 16 (previously presented): The circuit of claim 14 wherein the fourth and fifth transistors while switched on are connected to supply voltages substantially at the second and first power supply terminals to the control electrodes of the first and second transistors and the first and second capacitors, respectively.

Claim 17 (original): The circuit of claim 16 wherein all the transistors and capacitors are field effect devices.

Claim 18 (previously presented): The circuit of claim 17 wherein all the transistors and capacitors are included on an integrated circuit chip, the first and second resistive elements including first and second resistors on the chip.

Claim 19 (canceled).

Claim 20 (currently amended): A circuit comprising a first signal terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including a first transistor having a first conductivity type, the first transistor including a control electrode and a path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold, the path being connected in series across first and second opposite power supply terminals, an output terminal coupled to the path, pulse shaping circuitry connected between the first signal terminal and the control electrode for (a) causing the path of the transistor to be on and off while the voltage source has the first and second

levels; the pulse shaping circuitry including: (a) a switching circuit connected to be responsive to the voltage at the first terminal, the switching circuit including an output terminal that is DC connected to the control electrode of the first transistor; and (b) a capacitor connected between the control electrode and the first power supply terminal, the switching circuit including a resistive element for supplying current from the first power supply terminal to the control electrode of the first transistor and the capacitor while the voltage at the first signal terminal has the first level, the switching circuit being arranged for supplying a voltage substantially equal to the voltage at the second power supply terminal to (i) the control electrode of the first transistor and (ii) the capacitor while the voltage at the first signal terminal has the second level; the switching circuit comprising: a first inverter including second and third transistors respectively arranged to be switched on and off in response to the voltage at the first signal terminal respectively having first and second values, the first inverter including the resistive element for supplying current from the first power supply terminal to the control electrode of the first transistor and the capacitor while the second transistor is switched on; the second and third transistors being respectively of the first conductivity type and a second conductivity type opposite to the first conductivity type, each of the second and third transistors having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the second and third transistors are driven in parallel by the voltage at the first signal terminal, the output terminal of the inverter being between the source drain paths of the second and third transistors, the resistive element being connected between the source drain path of the third transistor and the output terminal of the inverter.

Claim 21 (previously presented): The circuit of claim 20 wherein the resistive element comprises a resistor.

Claim 22 (previously presented): The circuit of claim 14, wherein the first resistive element is connected between the source drain paths of the PFET and NFET of the first inverter, and the connection of the first resistive element to the PFET and NFET of the first inverter is such that substantial current flows through the first resistive element while the NFET of the first inverter is switched on and insubstantial current flows through the first resistive element while the NFET and PFET of the first inverter are respectively switched off and on, and the second resistive element is connected between the source drain paths of the PFET and NFET of the

second inverter and the connection of the first resistive element to the NFET and PFET of the second inverter is such that substantial current flows through the second resistive element while the PFET of the second inverter is switched on and insubstantial current flows through the second resistive element while the PFET and NFET of the second inverter are respectively switched off and on.

Claim 23 (previously presented): The circuit of claim 20, wherein the resistive element is connected between the source drain paths of the second and third transistors and the connection of the resistive element to the second and third transistors is such that substantial current flows through the resistive element while the third transistor is switched on and insubstantial current flows through the resistive element while the third transistor is switched off and the second transistor is switched on.

Claim 24 (previously presented): The circuit of claim 12, wherein the resistor is connected between the source drain paths of the PFET and NFET of the inverter, and the connection of the resistor to the PFET and NFET of the inverter is such that substantial current flows through the resistor while the NFET is switched on and insubstantial current flows through the resistor while the NFET is switched on and the PFET is switched off.

Claim 25 (previously presented): The circuit of claim 11, wherein the resistor is connected between the source drain path of the PFET of the inverter and the output terminal of the inverter.

Claim 26 (previously presented): The circuit of claim 25, wherein the resistor is connected between the source drain paths of the NFET and PFET of the inverter, and the connection of the resistor to the NFET and PFET of the inverter is such that substantial current flows through the resistor while the PFET is switched on and insubstantial current flows through the resistor while the PFET is switched on and the NFET is switched off.